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RTL-Based Modeling and Verification of a Three-Channel Package-Scale Galvanic Isolation Interface for Wide-Bandgap Gate Drivers

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Abstract
Wide-bandgap power switches require gate-driver interfaces that combine reinforced galvanic isolation, low propagation delay, diagnostic communication, and robust fault behavior. This paper presents an RTL-based digital and behavioral realization of a three-channel package-scale galvanic isolation interface inspired by RF-coupled co-packaged microantenna architectures. The proposed model separates the physical radio-frequency isolation barrier from its digital control plane and implements three independent paths: a direct controller-to-driver PWM channel, an edge-coded reverse power-control channel, and a half-duplex bidirectional diagnostic channel. The design additionally incorporates programmable channel delay, safe-low fault injection, transmitter mutual exclusion, timeout recovery, and a four-bit offset-calibration controller. The power-control channel encodes rising and falling PWM transitions using short and long pulses, respectively, while the receiver reconstructs the PWM state through pulse-width classification. The diagnostic controller uses a finite-state machine with idle, query, turnaround, response, and recovery states to prevent simultaneous transmission across a shared isolation channel. A self-checking Verilog testbench verifies forward and reverse communication, edge-code reconstruction, direction switching, channel-fault response, and calibration convergence. The resulting platform provides a synthesizable digital foundation for mixed-signal co-design, FPGA prototyping, and pre-silicon verification of package-scale isolation interfaces for SiC and GaN gate-driver applications.
Keywords: galvanic isolation, wide-bandgap gate driver, SiC, GaN, on-off keying, half-duplex communication, edge coding, Verilog, RTL verification, fault-tolerant interface.

1. Introduction

Silicon-carbide (SiC) MOSFETs and gallium-nitride (GaN) transistors enable higher switching frequency, lower switching loss, and reduced passive-component size in automotive, industrial, and renewable-energy converters. These benefits also increase the electrical stress imposed on the gate-driver interface. Fast drain-voltage transitions create large common-mode transients, while reinforced isolation requirements demand high surge withstand capability and low parasitic coupling between the low-voltage controller and the high-voltage power stage [1]-[4].

Conventional digital isolators use capacitive, transformer, or hybrid coupling barriers. Although these techniques provide mature solutions, the simultaneous achievement of compact integration, reinforced

isolation, high common-mode transient immunity, low propagation delay, and multiple independent channels remains challenging [5]-[9]. Package-scale isolation based on side-by-side co-packaged dice and near-field RF coupling offers an alternative. The physical distance through the molding compound supports a high isolation rating, and the small inter-die parasitic capacitance improves common-mode transient immunity [1], [10], [11].

A recent three-channel package-scale interface demonstrated a driver-control channel, a half-duplex diagnostic channel, and a power-control channel using RF-coupled microantennas and on-off-keyed carriers [1]. The reported silicon implementation validates the feasibility of combining three communication functions in a compact package. However, early architectural exploration and digital verification require an RTL-level representation that can be simulated rapidly, synthesized for FPGA prototyping, and subjected to systematic fault scenarios before analog and RF implementation.

This work develops such a model. The physical RF chain is abstracted as a timed digital channel, while the digital behavior is implemented using modular Verilog blocks. The main contributions are: a parameterized direct PWM channel; an energy-aware short/long edge-coding channel; a half-duplex diagnostic FSM with a guard interval and timeout recovery; a digital offset-calibration controller; safe-low fault handling; and a self-checking verification environment. The paper deliberately distinguishes between features implemented in RTL and properties that require transistor-level, electromagnetic, package, and high-voltage validation.

2. Literature Survey

Early galvanic isolators employed integrated transformers or capacitors to transfer digital information across a dielectric barrier. Transformer-based interfaces can achieve high data rate and good immunity, but their isolation rating and parasitic capacitance depend strongly on dielectric thickness, winding geometry, and package construction [5], [6]. Capacitive isolators offer compact implementation but require robust modulation and receiver architectures to reject common-mode transients [7]. Hybrid data-and-power systems have also used resonant transformers and LC barriers to combine isolated communication with power transfer [8], [9].

The migration to SiC and GaN devices has intensified the need for gate-driver isolation with high common-mode transient immunity. Fast switching edges can couple displacement current through the isolation capacitance and disturb the receiver decision circuit. Therefore, modern gate-driver interfaces must simultaneously control propagation delay, pulse-width distortion, false switching, and recovery from missing or corrupted communication [2]-[4].

Package-scale isolation replaces a thin on-chip dielectric barrier with a comparatively large inter-die spacing inside the package. RF-coupled planar microantennas have been used to demonstrate high isolation ratings while retaining a small two-chip system-in-package form factor [10]-[12]. A package-scale implementation in GaN technology demonstrated the suitability of planar electromagnetic coupling for gate-driver applications [11]. Spina et al. extended this principle to a three-channel BCD implementation containing independent driver-control, diagnostic, and power-control channels [1].

The use of on-off keying is attractive because the RF oscillator is active only when a logic one or coded pulse is transmitted. The direct PWM channel minimizes latency, whereas edge coding reduces average transmitter activity in a lower-bandwidth control loop. Half-duplex operation permits one antenna and one RF front end to support communication in both directions, but requires a guard interval and mutual-exclusion logic to prevent contention. These observations motivate the proposed RTL organization.[16],[17].

At the digital-design level, parameterized delay models, finite-state machines, counters, pulse-width classifiers, and self-checking testbenches provide an efficient mechanism for exploring communication timing and safety behavior. RTL cannot reproduce antenna coupling, RF amplitude, rectifier sensitivity, common-mode transient immunity, or surge withstand voltage. Nevertheless, it can verify sequencing, coding, timeout, calibration, fault response, and interface correctness before costly mixed-signal implementation.[18].

3. Proposed System Architecture

The proposed architecture models two isolated domains: the controller domain and the gate-driver domain. Three independent logical channels connect them. The driver-control channel transports the primary PWM gate command from controller to driver. The diagnostic channel supports controller queries and driver responses. The power-control channel transports a regulation PWM signal from the driver side to the controller side. The physical implementation may use 1.5-GHz carriers for the outer channels and a 0.5-GHz carrier for the middle diagnostic channel, following the frequency and physical separation strategy reported in [1].

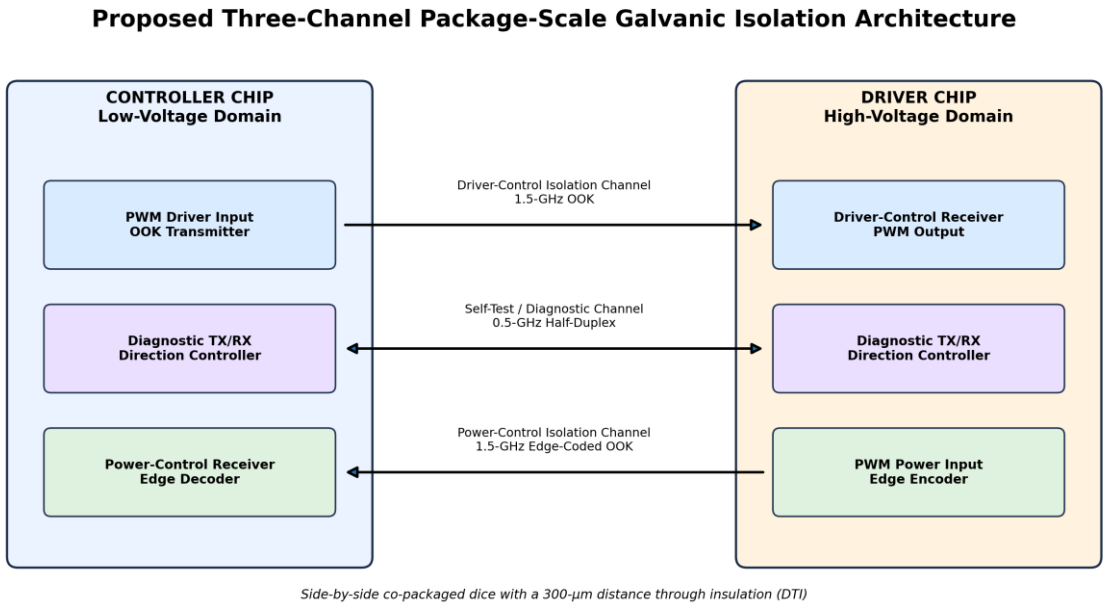

Figure 1. Proposed three-channel package-scale galvanic isolation architecture.

Channel	Direction	Physical concept	RTL block	Safety feature	Principal metric
Driver control	Controller → Driver	Direct OOK PWM	Programmable delay	Safe-low fault forcing	Propagation delay/PWD
Diagnostic	Bidirectional	0.5-GHz half-duplex	FSM + shared channel	Mutual exclusion and timeout	Turnaround/response time
Power control	Driver → Controller	Edge-coded OOK	Encoder + decoder	Invalid-pulse detection	Code separation and power activity
Calibration	Local receiver control	Offset cancellation	Up/down code search	Saturation termination	Calibration cycles

Table 1. Functional partition of the proposed RTL model.

4. Methodology

4.1 Isolation-Barrier and RF Abstraction

The package-scale barrier is represented conceptually by two dice separated by a distance through insulation, d_DTI. For a molding compound having dielectric strength E_d, an initial idealized withstand estimate is

$$V_{ISO,ideal} = E_d \, d_{DTI} \qquad (1)$$

This relation is not a substitute for reinforced-isolation qualification. Electric-field crowding, package geometry, aging, moisture, creepage, manufacturing variation, and the applicable surge standard must be considered during physical design. The resonance of each antenna-tank network is approximated by

$$f_{RF} = \frac{1}{2\pi\sqrt{L_{ANT} C_{TANK}}} \qquad (2)$$

The transmit-to-receive coupling loss is

$$T_{RX,L} = -20log_{10} | \frac{V_{RX}}{V_{TX}} | \ dB \qquad (3)$$

In the RTL platform, the oscillator, microantenna pair, rectifier, amplifier, and comparator are replaced by a parameterized cycle-delay channel. This abstraction preserves causality, configurable latency, and fault behavior while avoiding claims of RF accuracy.

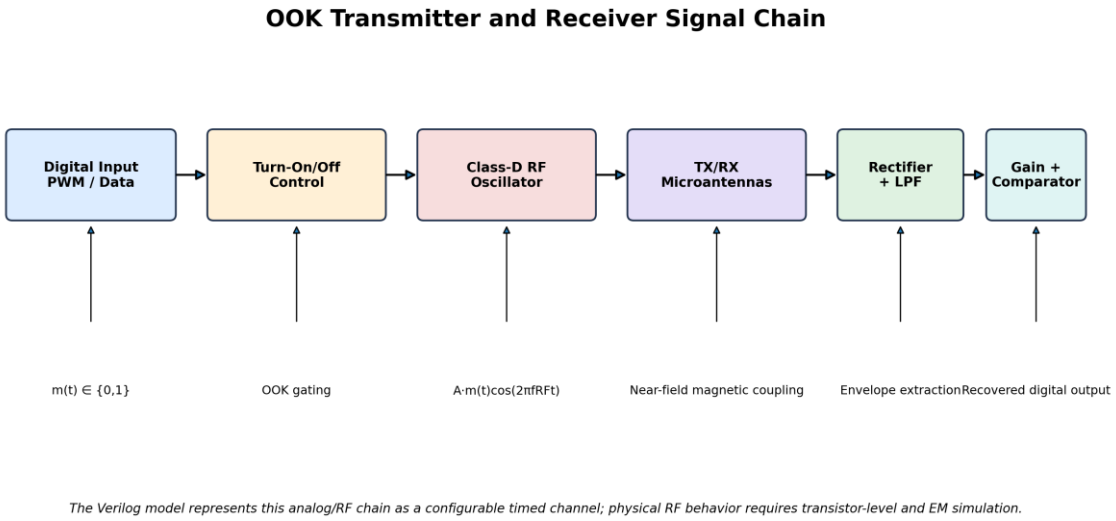

Figure 2. Physical OOK transmitter/receiver chain and its behavioral abstraction.

4.2 Direct Driver-Control Channel

The direct channel carries the gate-control PWM without coding. The input is shifted through a parameterized register chain, programmable by DRIVER_DELAY_CYCLES. A fault control overrides the delayed value and forces the output low, representing a conservative safe state when the isolation link is unavailable. If the clock period is T_CLK and the delay parameter is N_D, the modeled propagation delay is

$$t_{PD,model} = N_D\, T_{CLK} \qquad (4)$$

For separate input and output edge measurements, the rising and falling propagation delays are

$$t_{PD,r} = t_{OUT,r} - t_{IN,r} \qquad (5)$$

$$t_{PD,f} = t_{OUT,f} - t_{IN,f} \qquad (6)$$

The pulse-width distortion is

$$\boldsymbol{PWD} = |\, \boldsymbol{T_{HIGH,out}} - \boldsymbol{T_{HIGH,in}} \,| \qquad (7)$$

4.3 Power-Control Edge Encoder

The reverse power-control channel reduces transmitter activity by encoding only PWM transitions. The power_edge_encoder module stores the previous PWM state. A 0-to-1 transition starts a short coded pulse, whereas a 1-to-0 transition starts a long coded pulse. While a coded pulse is active, encoder_busy prevents a new pulse from being launched.

$$T_{CODE} = T_{SHORT} \textit{for a rising edge} \qquad (8)$$

$$T_{CODE} = T_{LONG} \textit{for a falling edge} \qquad (9)$$

For a synchronous implementation, the coded widths are integer multiples of T_CLK:

$$T_{SHORT} = N_S\, T_{CLK}, T_{LONG} = N_L\, T_{CLK} \qquad (10)$$

The separation between the two pulse classes must exceed timing uncertainty:

$$T_{LONG} - T_{SHORT} > 2\left(T_{JITTER} + T_{QUANT} + T_{MARGIN}\right) \qquad (11)$$

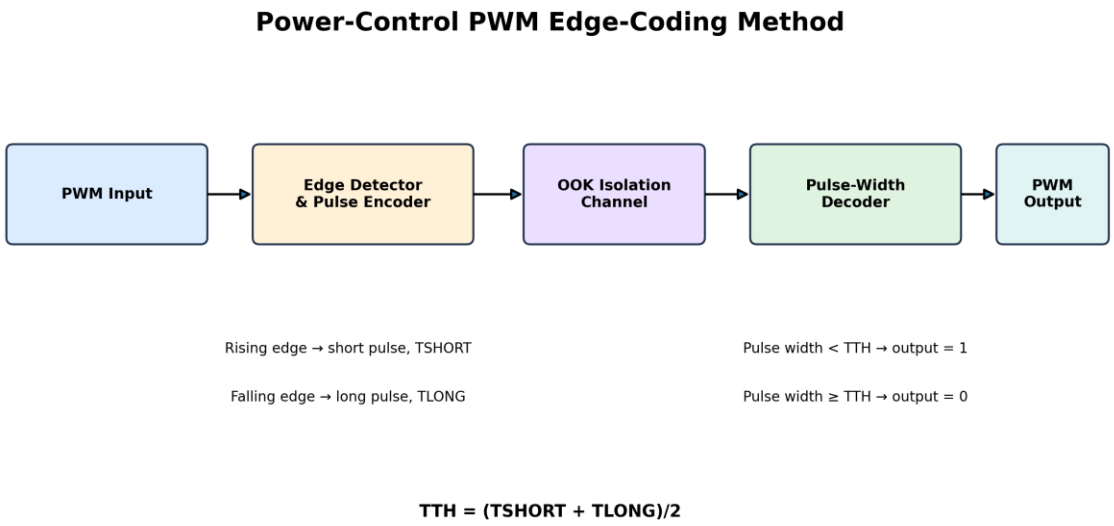

Figure 3. Short/long pulse edge-coding method used by the power-control channel.

4.4 Power-Control Edge Decoder

The power_edge_decoder module counts the number of clock cycles for which coded_pulse remains high. At the falling edge of the coded pulse, the measured width is compared with MIN_VALID_WIDTH and WIDTH_THRESHOLD. A pulse shorter than the minimum is rejected and raises pulse_error. A valid pulse below the threshold sets the reconstructed PWM output high, whereas a pulse at or above the threshold clears it.

$$N_{TH} = \frac{N_S + N_L}{2} \qquad (12)$$

$$PWM_{OUT} = 1, N_{VALID} \leq N_P < N_{TH} \qquad (13)$$

$$PWM_{OUT} = 0, N_P \geq N_{TH} \qquad (14)$$

The decoder therefore performs both edge interpretation and basic crosstalk rejection. The digital margin against a spurious pulse of width N_XT is*)*

$$\boldsymbol{M_{XT} = N_{VALID} - N_{XT}} \qquad (15)$$

4.5 Half-Duplex Diagnostic Channel

The half_duplex_channel module selects either controller_tx_data or driver_tx_data according to the direction signal. The selected data is passed through a parameterized delay model and routed only to the receiving side. The inactive receiver output is held low. Channel-fault injection forces both reconstructed receive paths to the safe state.

The diagnostic_control_fsm module sequences five operational conditions: IDLE, QUERY, GUARD, RESPONSE, and ERROR. In IDLE and QUERY, only the controller transmitter is enabled. In GUARD, both transmitters are disabled. In RESPONSE, only the driver transmitter is enabled. An expired timeout transfers control to ERROR before the controller-default direction is restored.

TX_EN,CTRL · TX_EN,DRV = 0 (16)

T_GUARD = N_G T_CLK (17)

T_TIMEOUT = N_TO T_CLK (18)

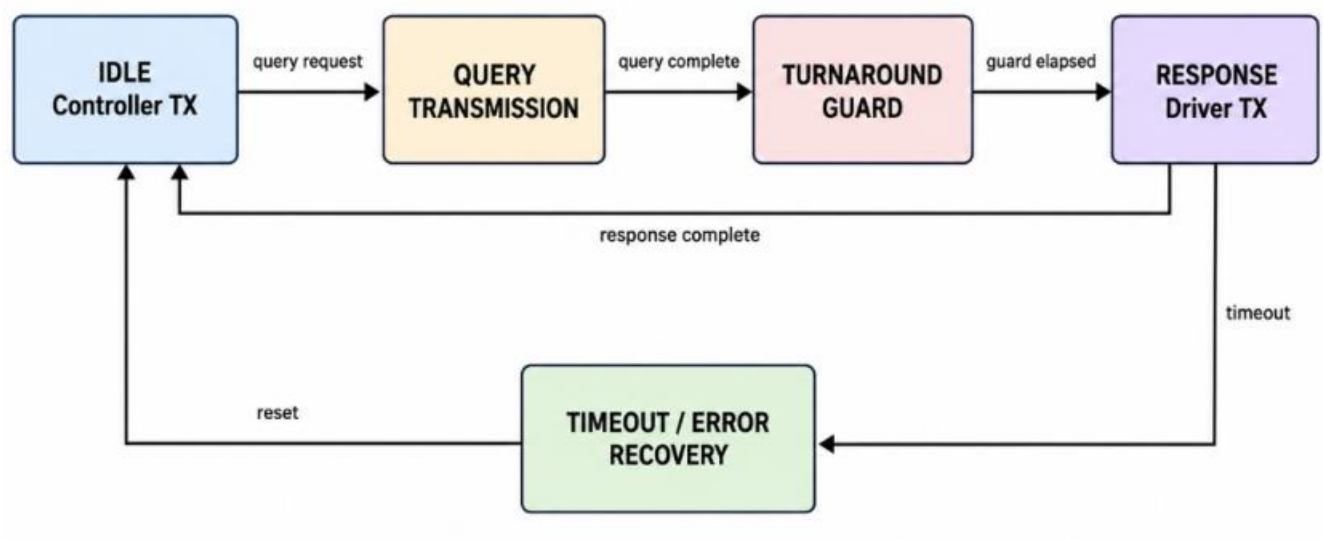

Figure 4. Half-duplex diagnostic channel control sequence.

4.6 Offset-Calibration Controller

The offset_calibration_controller module abstracts the receiver offset-cancellation process. At calibration_start, the controller stores comparator_sign and initializes a four-bit code. If the initial sign is positive, the code decrements; if negative, it increments. Calibration terminates when the comparator sign reverses or the code reaches an endpoint. For an N-bit code and calibration clock f_CAL, the worst-case search time is

$$T_{CAL,max} = (2^N - 1)/f_{CAL} \quad (19)$$

The calibration_done and calibration_active outputs support system-level sequencing and permit the testbench to verify convergence.

4.7 Integrated RTL Top Level

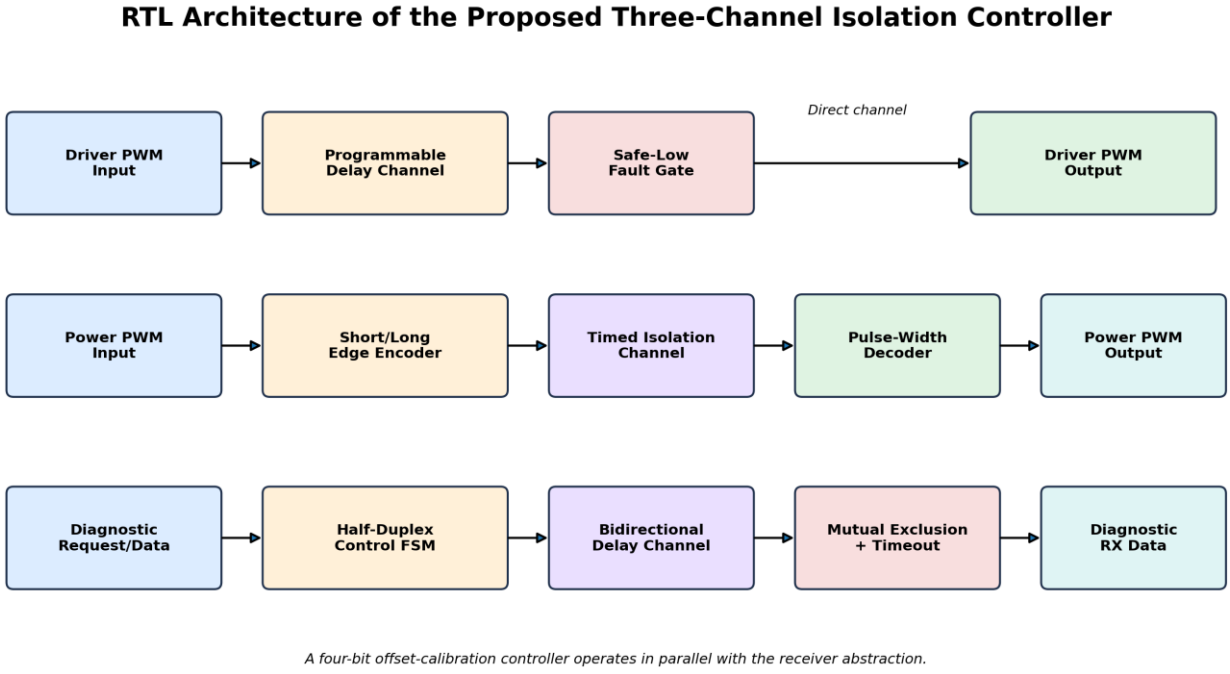

Figure 5. Modular RTL architecture of the implemented three-channel controller.

The top-level module instantiates the programmable delay, edge encoder, edge decoder, diagnostic FSM, half-duplex channel, and offset-calibration controller as separate reusable units. Parameter values define the modeled channel delays, short and long coded-pulse widths, decoder threshold, turnaround guard interval, and timeout interval. This modular structure permits independent synthesis, verification, and replacement of each subsystem.

5. Verilog Implementation

The design is written in Verilog-2001 and uses synchronous active-low reset. The implementation avoids non-synthesizable timing controls inside the design modules. Only the testbench contains clock-generation delays, tasks, display statements, and waveform-dump commands. The principal parameters used in the supplied testbench are listed in Table 2.

Parameter	Configured value	Interpretation
DRIVER_DELAY_CYCLES	3	Direct-channel latency
POWER_DELAY_CYCLES	2	Coded-channel transport latency
DIAG_DELAY_CYCLES	2	Bidirectional diagnostic latency
SHORT_PULSE_CYCLES	3	Encoded rising-edge width
LONG_PULSE_CYCLES	7	Encoded falling-edge width
WIDTH_THRESHOLD	5	Short/long classification boundary
GUARD_CYCLES	3	Half-duplex turnaround interval
TIMEOUT_CYCLES	40	Maximum query or response duration
Calibration code width	4 bits	Maximum of 15 search steps

Table 2. RTL parameters used in the supplied verification configuration.

The programmable delay module uses a shift register whose length is controlled by DELAY_CYCLES. The edge encoder uses previous-state detection and a pulse counter. The edge decoder uses a width counter and a falling-edge detector. The diagnostic FSM uses localparam state encodings and separate sequential and combinational processes. The calibration controller uses a bounded code search. These structures are suitable for FPGA or ASIC synthesis, subject to normal timing constraints and technology-specific optimization.

6. Verification Environment

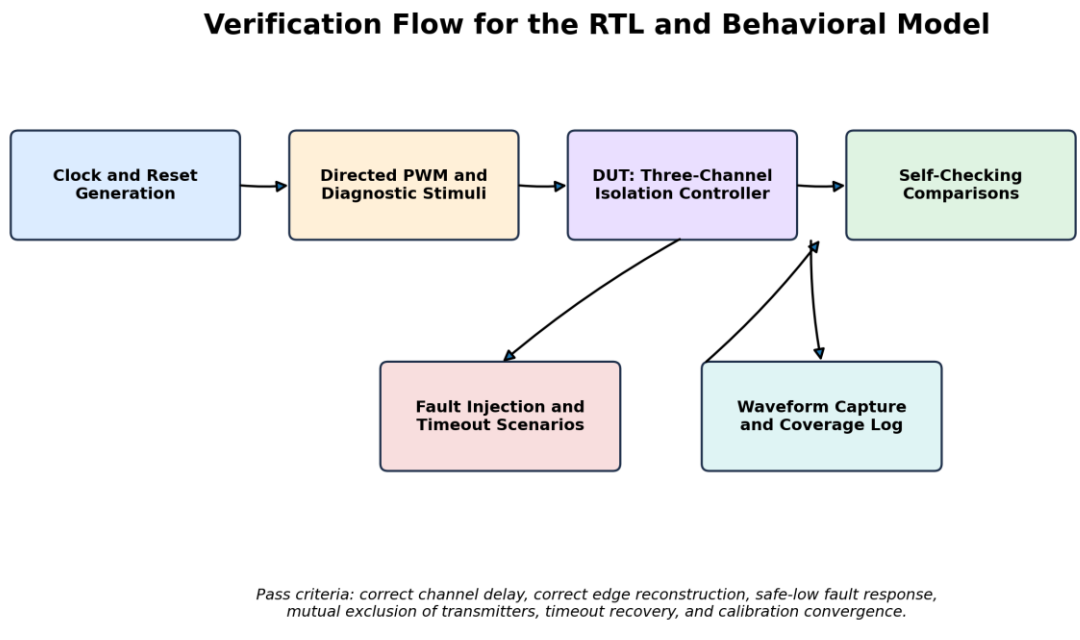

Figure 6. Self-checking verification flow for the proposed RTL model.

A self-checking Verilog testbench generates a 100-MHz clock and applies reset before beginning directed tests. The testbench records a VCD waveform and uses a check_result task to compare observed conditions with expected behavior. Failures increment error_count, while successful checks are reported as PASS messages.

Test	**Stimulus**	**Expected response**	**Verified property**
Reset	rst_n asserted then released	All controls return to defaults	Deterministic startup
Driver channel	PWM high and low	Delayed output follows input	Forward communication
Power rising edge	PWM 0→1	Short code sets output high	Encoder/decoder operation
Power falling edge	PWM 1→0	Long code clears output	Width classification
Diagnostic query	Controller TX enabled	Driver receives data	Forward half-duplex path

Test	Stimulus	Expected response	Verified property
Turnaround	Query complete	Guard then direction reversal	Contention avoidance
Diagnostic response	Driver TX enabled	Controller receives data	Reverse half-duplex path
Mutual exclusion	Observe TX enables	Never simultaneously high	Safety invariant
Channel fault	Force driver fault	Output forced low	Fail-safe response
Calibration	Change comparator sign	calibration_done asserted	Search convergence

Table 3. Directed tests implemented in the supplied testbench.

The current testbench verifies representative functional scenarios. A complete verification campaign should additionally randomize delay parameters, inject malformed pulse widths, force diagnostic timeout, test calibration saturation, toggle faults during active transactions, and collect code and functional coverage. Assertions may be added for mutual exclusion, bounded calibration completion, pulse-width validity, and safe-state recovery.

7. Results and Discussion

1. Synthesized Device View

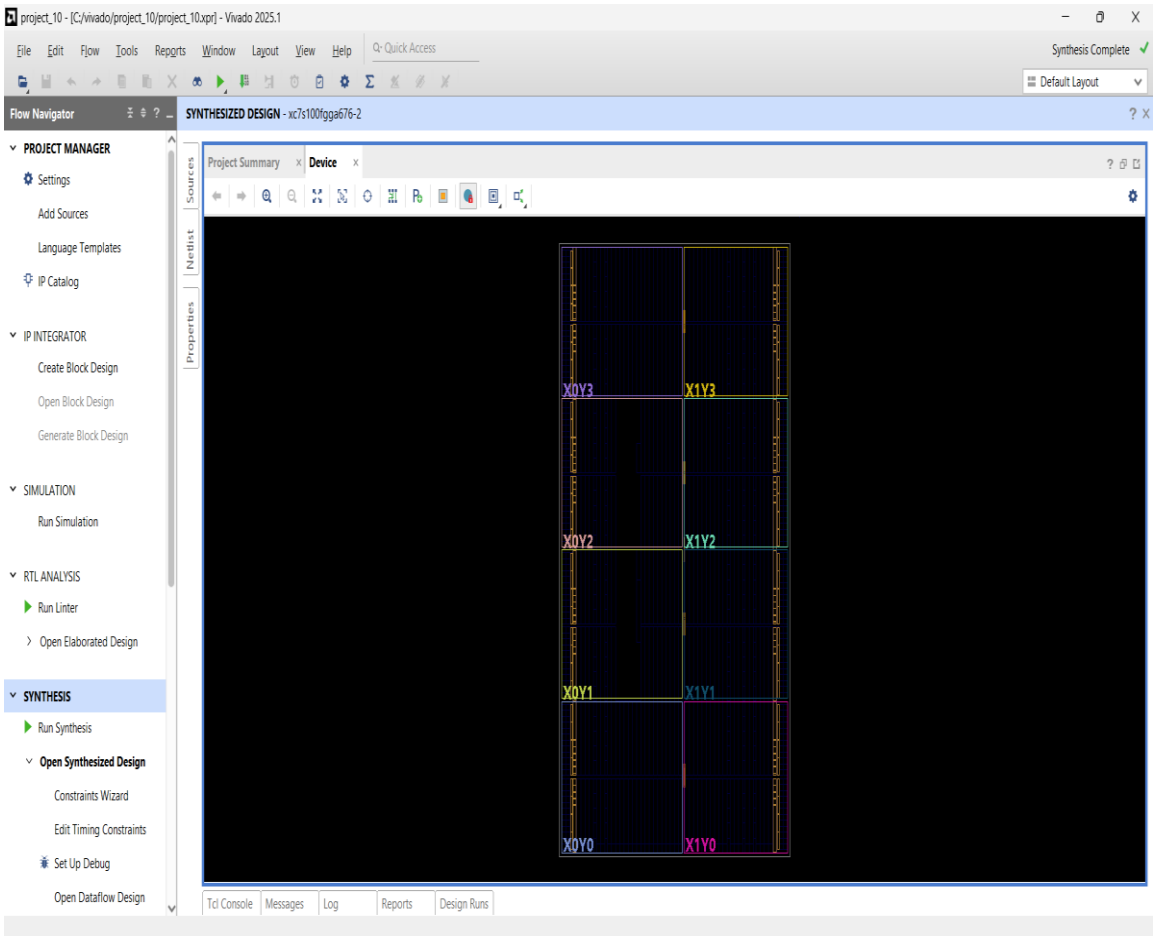

Figure 1. Synthesized device view of the target Spartan-7 FPGA.

Figure 1 shows that synthesis completed successfully and the synthesized design was opened for the selected Spartan-7 device. The device floorplan is divided into clock regions labelled X0Y0 through X1Y3. The successful device view indicates that Vivado generated a valid synthesized netlist compatible with the selected FPGA family and package.

At this stage, the image does not show final placement and routing. Therefore, it should be interpreted as evidence of successful synthesis and device targeting rather than as a post-implementation floorplan. Final timing closure, routing congestion, clock placement, and implemented resource distribution must be evaluated after running implementation.

2. Synthesis Status and Tool Report

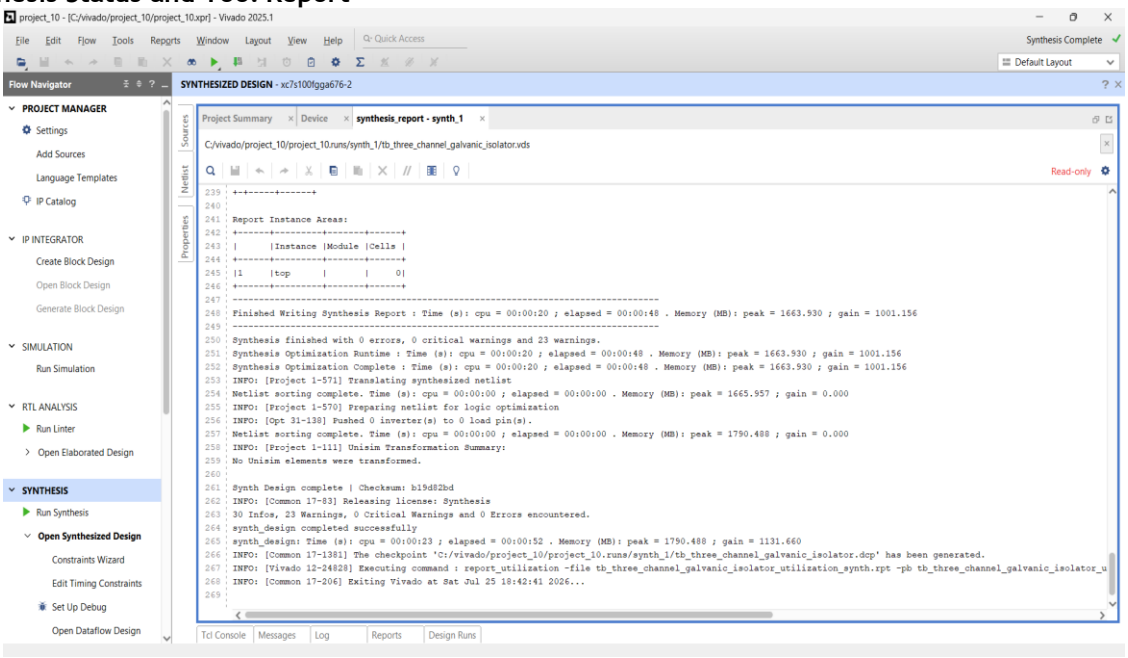

Figure 2. Vivado synthesis completion report.

The synthesis log reports zero errors and zero critical warnings, confirming that the RTL was accepted by the synthesis engine and converted into a synthesized netlist. Twenty-three warnings are present. Since the warning details are not visible in the supplied image, they should be reviewed individually before hardware programming. Typical warnings may relate to unused signals, constant logic, unconstrained paths, incomplete timing constraints, or testbench-related hierarchy.

The displayed instance-area section reports zero cells for the shown top instance, while the elaborated schematic in a separate image reports 11 cells and 36 nets. This difference strongly suggests that the synthesis run may have used a testbench-oriented top-level or that optimization removed inactive logic under the selected hierarchy. The project top-module assignment and source-set configuration should therefore be checked before using the utilization report as a final hardware-resource result.

3. Power Estimation

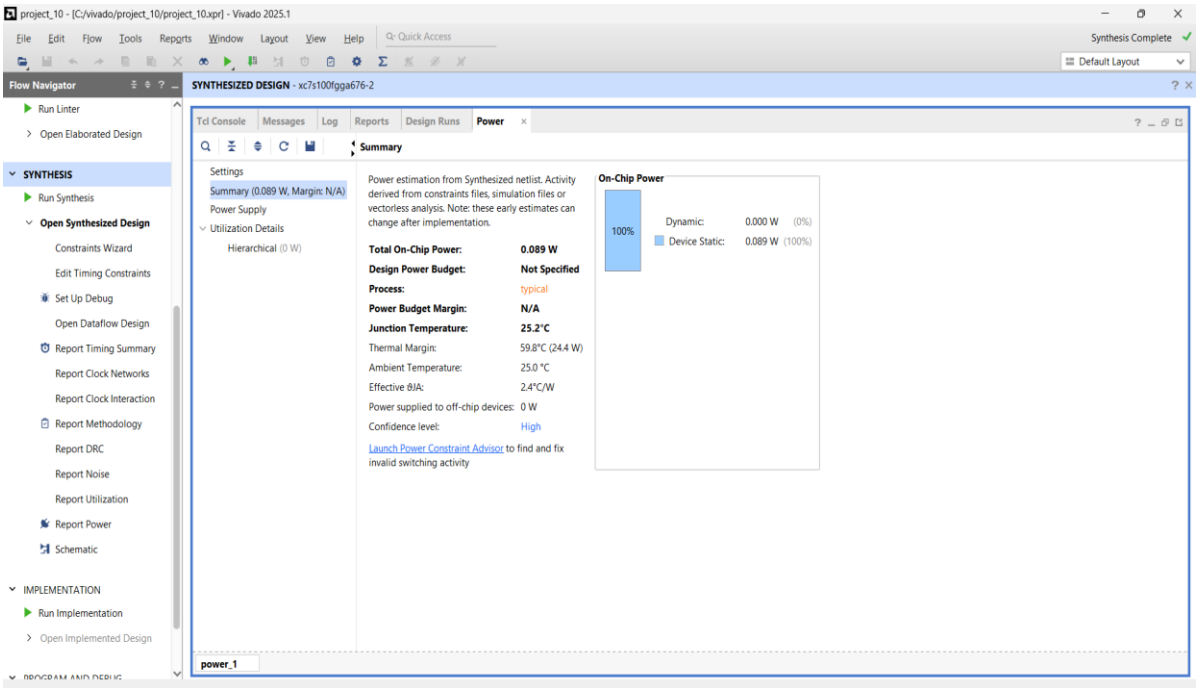

Figure 3. Early synthesized-netlist power estimate.

The synthesized-netlist power report estimates a total on-chip power of 0.089 W. The complete estimate is attributed to device static power, while dynamic power is reported as 0.000 W. This does not necessarily

indicate that the active design consumes no switching power. It indicates that representative switching activity, clocks, or implementation-derived activity information was not available to the early power-estimation stage.

The reported junction temperature is 25.2 °C for an ambient temperature of 25.0 °C, with a large thermal margin. These values are favourable for the current early estimate. However, a realistic power result requires valid clock constraints, correct signal-toggle rates, post-implementation routing data, and preferably switching activity imported from simulation. Consequently, the 0.089 W value should be presented as a preliminary static-dominated estimate rather than the final operating power of the complete galvanic-isolation system.

The analogue/RF sections of the intended physical system, including the class-D oscillators, antenna tanks, rectifiers, amplifiers, and comparators, are not represented by the FPGA power report. Their power must be determined separately through circuit simulation or silicon measurement.

4. RTL Elaborated Schematic

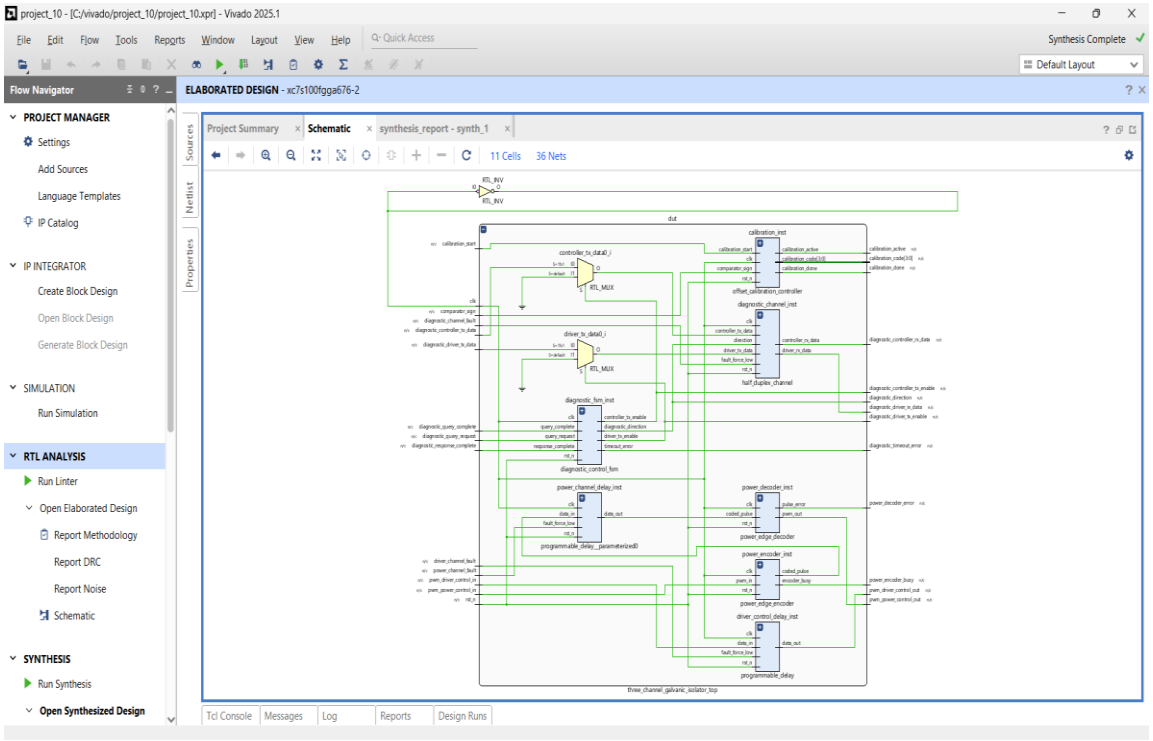

Figure 4. Elaborated RTL schematic of the integrated isolation-control architecture.

Figure 4 confirms the structural integration of the major digital modules. The schematic identifies an offset_calibration_controller, a half_duplex_channel, a diagnostic_control_fsm, a power_edge_encoder, a power_edge_decoder, and two programmable_delay blocks associated with the driver-control and power-control paths. The Vivado schematic header reports 11 cells and 36 nets for the elaborated design.

The calibration controller receives calibration_start and comparator_sign inputs and produces calibration_active, calibration_code, and calibration_done outputs. This structure supports the iterative offset-compensation methodology. The half-duplex diagnostic channel connects controller and driver data signals and exposes direction and transmitter-enable outputs. The associated diagnostic control FSM manages query completion, response completion, guard timing, and timeout behaviour.

The reverse power-control path contains an encoder that converts PWM transitions into coded pulses and a decoder that reconstructs the PWM state. The programmable delay blocks provide a behavioural representation of the physical isolation-channel delay and include fault-forcing inputs. This modular organization supports independent verification of each channel and simplifies later substitution of more accurate mixed-signal channel models.

The visible interconnection between modules demonstrates that the complete design is not merely a collection of isolated blocks. The calibration, diagnostic, driver-control, power-control, fault, reset, and clock signals are connected at top level, enabling system-level behavioural verification.

5. Behavioural Simulation

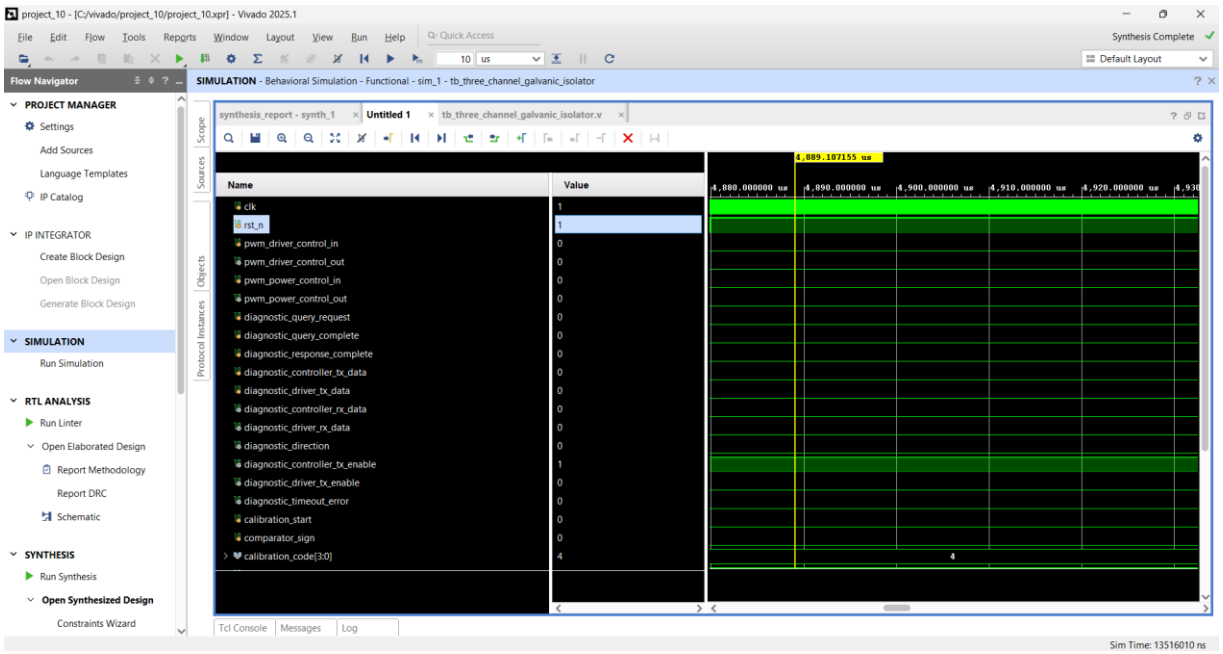

Figure 5. Behavioural simulation waveform at approximately 4.889 ms.

The behavioural waveform shows the design in a stable operating interval at approximately 4.889 ms. Reset is deasserted, indicating normal operation. At the cursor position, the driver-control input and output are both low, and the power-control input and output are also low. The diagnostic request, query-complete, and response-complete signals are inactive.

The diagnostic controller transmitter enable is high while the driver transmitter enable is low. This is consistent with the default controller-to-driver direction and satisfies the mutual-exclusion requirement that both diagnostic transmitters must not be active simultaneously. The timeout-error signal is low, indicating that no diagnostic timeout is present at the observed instant.

The calibration_start signal is low and the displayed calibration code is 4. This indicates that the calibration controller is not actively searching at the selected cursor position and is retaining a valid calibration value. The screenshot does not expose the entire calibration interval, so calibration convergence time and code-transition behaviour should be measured from a zoomed waveform covering reset and calibration start.

Because the captured interval is an idle portion of the waveform, it confirms stable quiescent behaviour but does not by itself demonstrate all rising-edge, falling-edge, encoded-pulse, direction-turnaround, timeout, and fault-injection cases. Those results should be documented using additional waveform captures showing active PWM transfer, short/long edge-code generation, decoder reconstruction, diagnostic turnaround guard time, timeout recovery, and safe-state forcing.

8. Conclusion

This paper presented a modular RTL-based model and verification framework for a three-channel package-scale galvanic isolation interface intended for wide-bandgap gate drivers. The architecture separates the physical RF isolation barrier from the digital communication and safety functions. A direct PWM channel supports low-latency gate control, a short/long pulse encoder and decoder support energy-aware reverse power control, and a half-duplex FSM supports bidirectional diagnostic communication with mutual exclusion, guard time, timeout recovery, and fault handling. A bounded digital calibration controller models receiver offset compensation. The supplied Verilog modules and self-checking testbench establish a reusable platform for FPGA prototyping and mixed-signal co-design. Future work should connect the digital model to transistor-level RF front ends, electromagnetic antenna models, package parasitics, and measured CMTI and surge-isolation data.

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