



Efficient VLSI Implementation of Hybrid LDPC-STBC Codes for Enhanced Satellite Communication Systems

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ABSTRACT

Satellite communication systems require reliable and hardware-efficient error control techniques because the transmitted data is commonly affected by noise, fading, interference and attenuation. This paper presents an efficient VLSI implementation of a hybrid Low-Density Parity-Check (LDPC) and Space-Time Block Coding (STBC) scheme for enhanced satellite communication systems. The methodology follows a two-level coding approach in which LDPC coding provides strong error correction through sparse parity-check based encoding and iterative decoding, while STBC improves link reliability by exploiting spatial diversity in multiple-antenna transmission. The design is implemented and evaluated using Xilinx Vivado on a Zynq-7000 device. The results taken from the thesis show that, for $N = 32$, the proposed method reduces LUT utilization from 104 to 6, total power from 34.692 W to 17.134 W and total delay from 18.142 ns to 14.766 ns. For $N = 64$, LUT utilization is reduced from 208 to 13 and total power is reduced from 69.384 W to 25.69 W. The results demonstrate that the hybrid LDPC-STBC architecture provides a compact and energy-efficient VLSI solution for reliable satellite communication.

Keywords: LDPC, STBC, VLSI, satellite communication, error correction code, Xilinx Vivado, Zynq-7000

I. INTRODUCTION

Error correction codes are essential in digital communication systems because they protect transmitted information from errors introduced by channel noise, interference and hardware limitations. In satellite communication, these problems are more critical because long-distance links are affected by fading, attenuation and limited power availability. Conventional error correction schemes such as Hamming, Golay and BCH codes are useful for basic error detection and correction, but they may not provide an efficient balance between reliability, hardware area, power and delay for modern high-data-rate satellite links.

LDPC codes are widely used because of their near-capacity error correction performance and suitability for parallel hardware implementation. STBC improves the reliability of wireless links by transmitting coded symbols across multiple antennas and time slots. The hybridization of LDPC and STBC therefore provides both coding gain and diversity gain. In this work, the methodology and numerical results are taken from the supplied thesis document. The objective is to convert the thesis content into a concise research paper with fewer headings, using the same proposed architecture, implementation platform and result values.

II. METHODOLOGY

The proposed methodology combines LDPC encoding and decoding with STBC encoding and decoding. In the LDPC stage, the input data vector is processed using a generator matrix to generate an encoded codeword. The thesis represents the encoding operation as $C = V \times G$, where V is the input data vector and G is the generator matrix. The generated codeword contains both the original information bits and parity bits. These parity bits introduce controlled redundancy, allowing the receiver to detect and correct errors that occur during transmission.

At the receiver side, syndrome calculation is used to identify the presence and location of errors. The received codeword is multiplied with the transpose of the parity-check matrix, represented as $S = R \times H^T$. If the syndrome is zero, the received word satisfies the parity-check equations. If the syndrome is non-zero, the decoder uses the syndrome information to locate the error and correct the received codeword. This process is suitable for hardware implementation because the sparse LDPC matrix reduces computational complexity and supports efficient logic realization.

The STBC part of the methodology improves communication reliability by exploiting spatial diversity. In the STBC encoder, symbols are arranged in a space-time structure and transmitted through multiple antennas over different time slots. This arrangement allows the receiver to combine multiple faded versions of the signal and recover the original symbols with improved reliability. The thesis also describes the use of Recursive Systematic Convolutional coding and MAP-based decoding principles within the STBC process for improving error recovery under noisy channel conditions.

The hybrid LDPC-STBC encoder performs two-stage coding. First, LDPC encoding generates parity bits and produces an encoded codeword. Second, the LDPC-encoded symbols are passed to the STBC encoder and transmitted across multiple antennas and time intervals. The decoder performs the reverse operation: the received encoded stream is split, the STBC decoder estimates the transmitted symbols, and the LDPC decoder performs iterative error correction using soft information feedback. This combination improves Bit Error Rate performance, reduces the effect of fading and supports reliable data transmission in noisy satellite communication channels.

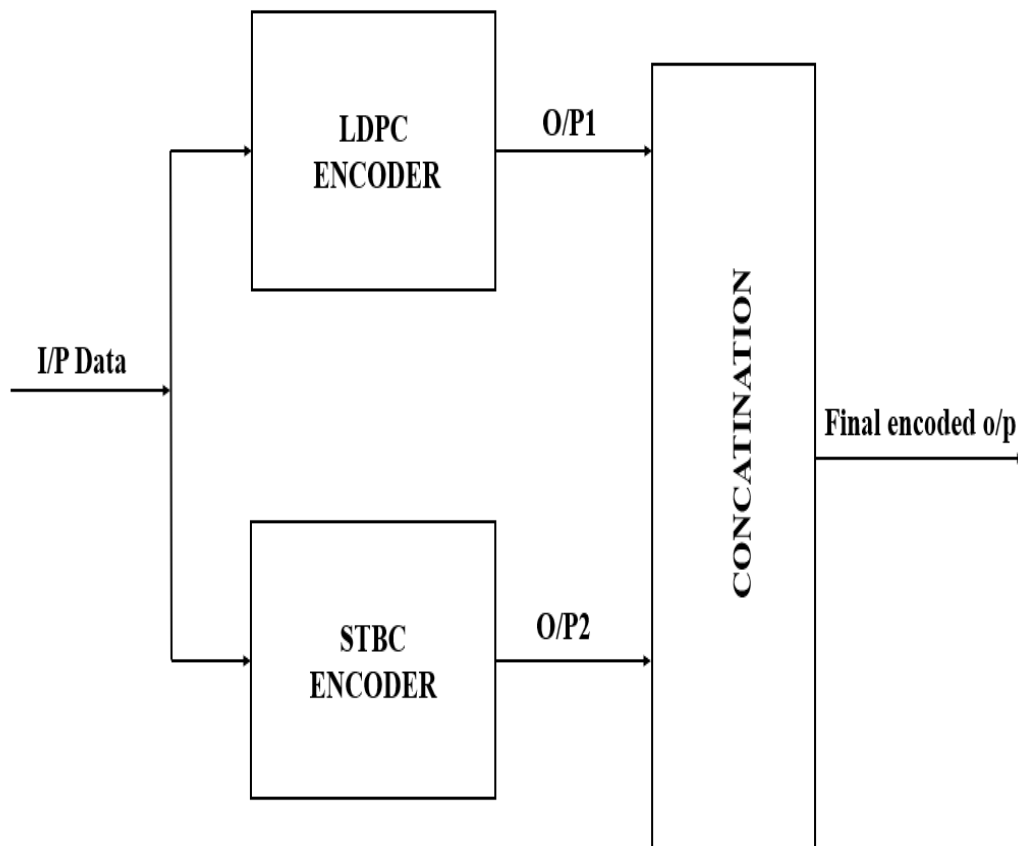


Fig. 1. LDPC-STBC encoder architecture used in the thesis methodology.

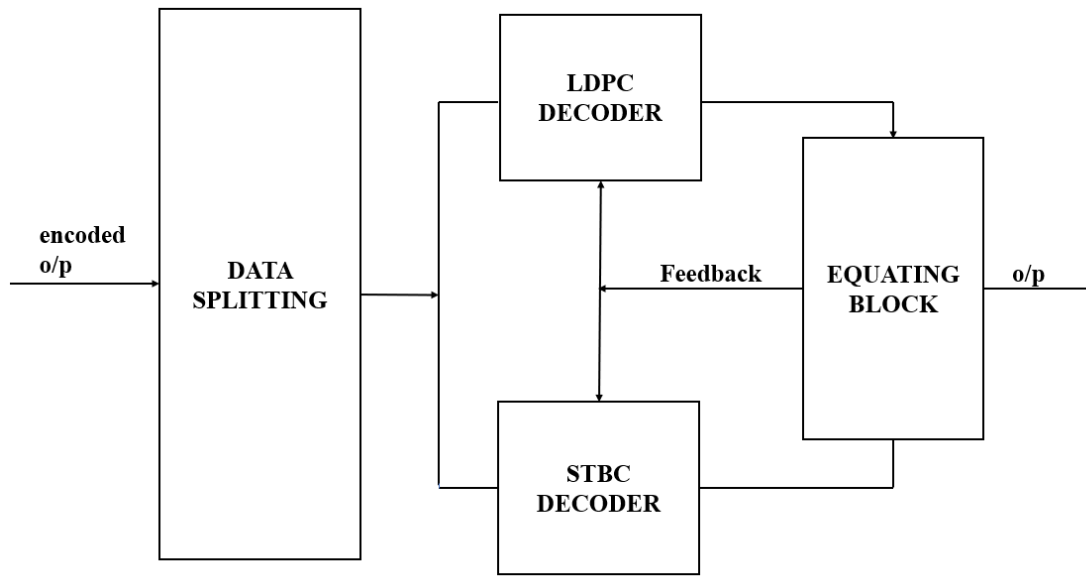


Fig. 2. LDPC-STBC decoder architecture used in the thesis methodology.

Table I. Implementation device specification used for synthesis

Parameter	Specification
Part Number	xc7z007sclg400-1
Family	Zynq-7000
Package	clg400
Speed Grade	-1
Temperature Grade	C

III. RESULTS AND DISCUSSION

The experimental results are reproduced from the thesis results section. The existing method for $N = 32$ can correct only one bit and fails when more than one error bit is present. In the proposed result for $N = 32$, the number of redundant bits is 16, the input applied is 113, the codeword is 485331304561, the error pattern after transmission is 5476, and the data is corrected without errors. The proposed area, power and delay values are compared with the existing method for $N = 16$, $N = 32$ and $N = 64$.

Table II. Performance comparison of existing and proposed methods for $N = 16$

Metric	Existing Method	Proposed Method	Comparison
LUT	52	3	94.2%
IO	70	96	37%
TOTAL POWER	17.346 W	8.985 W	48%
STATIC POWER	0.150 W	0.137 W	8.6%
DYNAMIC POWER	17.195 W	8.848 W	48.5%
TOTAL DELAY	9.701	15.011	54.7%
LOGIC DELAY	2.261	3.908	72.84%
NET DELAY	6.81	11.103	63.03%

For $N = 16$, LUT usage is reduced from 52 to 3 and total power is reduced from 17.346 W to 8.985 W. Static power decreases from 0.150 W to 0.137 W, while dynamic power decreases from 17.195 W to 8.848 W. The thesis result also shows a delay trade-off for this case, where total delay increases from 9.701 to 15.011, logic delay increases from 2.261 to 3.908 and net delay increases from 6.81 to 11.103. Thus, the $N = 16$ case gives strong area and power savings with increased delay.

Table III. Performance comparison of existing and proposed methods for N = 32

Metric	Existing Method	Proposed Method	Improvement
LUT Utilization	104	6	94% reduction
I/O Utilization	140	112	20% reduction
Total Power	34.692 W	17.134 W	50.6% reduction
Static Power	0.301 W	0.165 W	45.18% reduction
Dynamic Power	34.391 W	16.969 W	50.65% reduction
Total Delay	18.142 ns	14.766 ns	18.6% reduction
Logic Delay	4.522 ns	4.270 ns	5.57% reduction
Net Delay	13.620 ns	10.496 ns	22.93% reduction

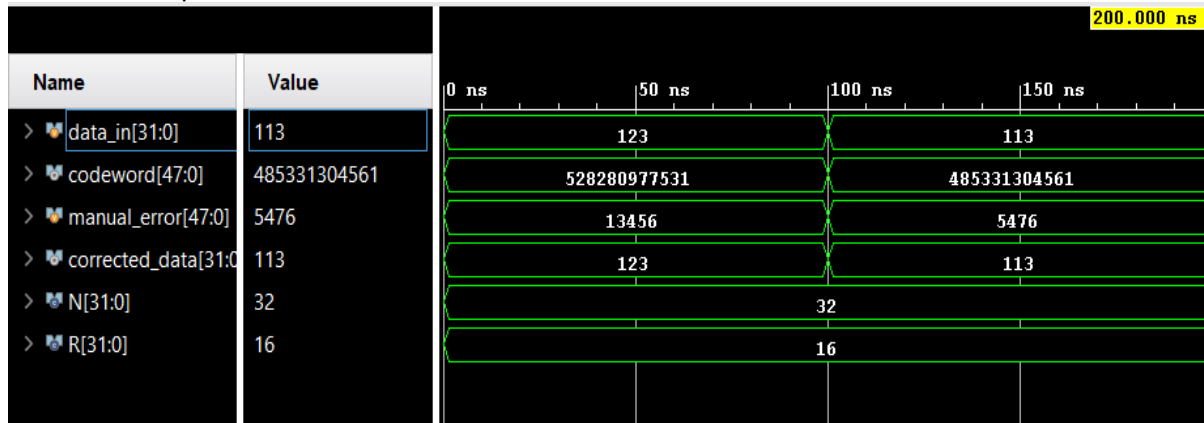
For N = 32, the proposed architecture gives clear improvement in area, power and delay. LUT utilization is reduced by 94%, I/O utilization is reduced by 20%, total power is reduced by 50.6%, static power is reduced by 45.18% and dynamic power is reduced by 50.65%. The total delay is reduced from 18.142 ns to 14.766 ns, giving an 18.6% reduction. Logic delay and net delay also decrease by 5.57% and 22.93%, respectively.

Table IV. Performance comparison of existing and proposed methods for N = 64

Metric	Existing Method	Proposed Method	Comparison
LUT	208	13	93.75%
IO	240	208	13.33%
TOTAL POWER	69.384 W	25.69 W	62.97%
STATIC POWER	0.602 W	0.215 W	64.28%
DYNAMIC POWER	68.782 W	25.475 W	62.96%
TOTAL DELAY	36.284	13.611	62.48%
LOGIC DELAY	9.044	3.944	56.39%
NET DELAY	27.24	9.667	64.5%

For N = 64, the proposed method shows the highest overall improvement. LUT usage is reduced from 208 to 13, corresponding to a 93.75% reduction, and I/O utilization is reduced from 240 to 208. Total power decreases from 69.384 W to 25.69 W, giving a 62.97% power reduction. The delay results also improve significantly: total delay decreases by 62.48%, logic delay decreases by 56.39% and net delay decreases by 64.5%. These values confirm that the proposed hybrid LDPC-STBC implementation is more efficient than the existing method for larger input sizes.

Overall, the thesis results indicate that the proposed architecture reduces LUT count and power consumption across all tested values of N. The most consistent improvements are observed for N = 32 and N = 64, where both power and delay are reduced. The N = 16 case demonstrates a power-area optimized design but involves a delay increase. Therefore, the proposed system is especially suitable for satellite communication systems where area and power efficiency are important and where scalable coding performance is required.

**Figure 3. Proposed Simulation Results for N=32**

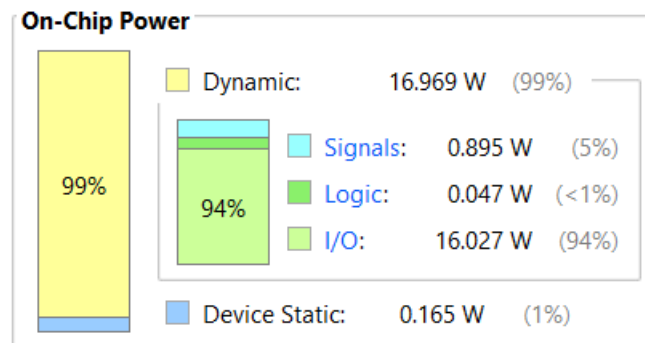


Figure 4. Proposed Power for N=32

IV. CONCLUSION

This paper presented a concise research version of the thesis work on efficient VLSI implementation of hybrid LDPC-STBC codes for satellite communication systems. The methodology combines LDPC-based error correction with STBC-based spatial diversity to improve communication reliability under noisy and fading channel conditions. The implementation results taken from the thesis demonstrate significant reduction in LUT utilization and power consumption, particularly for $N = 32$ and $N = 64$. For $N = 64$, the proposed system reduces LUT usage by 93.75%, total power by 62.97% and total delay by 62.48%. Hence, the hybrid LDPC-STBC approach provides an effective and hardware-efficient solution for enhanced satellite communication systems.

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